RF-SiP Design and Integration

Bergi Bagdasarian – Wireless Networking Group, Intel Corporation
Joe Blonski – Wireless Networking Group, Intel Corporation
Nozad Karim - Advance Product Development Group, Amkor Technology
Jingkun Mao - Advance Product Development Group, Amkor Technology
Email: nakri@amkor.com www.amkor.com

Abstract

The requirement to modularize the cell phone and other handset devices was initially driven by the objective of simplifying the platform level development of the radio frequency section and of improving the high volume manufacturability. To facilitate the high paced demand for miniaturization and integration of the RF portion of the wireless subsystem, Amkor Technology and Intel Corporation have started to engage in using SiP *(System in Package)* technology for new RF products. This initiated the development of a complete design chain flow involving package development using integrated and overmolded RF shielding, RF circuit design with integrated components, specialized testing, and assembly processes.

Both parties have aligned their efforts to continually optimize their respective RF-SiP designs. Both parties' system engineers, circuit designers, RF Silicon engineers, layout specialists, RF test engineers, and manufacturing teams have engaged to work together in an optimized design environment. The SiP design team was challenged with miniaturization, cost reductions, performance enhancements, high volume manufacturability, and shortened design cycles. This paper provides an overall RF subsystem high level overview and it discusses in detail the frequency domain response of embedded passive filters in a multilayer low cost organic substrate. It also illustrates how the measured data is combined with accurate full wave 3D simulation, for enhanced tool calibration and design optimization.

I. Introduction:

Due to the increasing complexity and miniaturization of today's wireless products, the radio subsystems are being driven to very aggressive trends in advanced silicon processes and higher levels of integration. The size constraints affect not only the subsystem's total footprint, but also the Z-height dimension, imposing restrictions achievable only through high levels of package integration. Even then, component selection remains a challenge, since all discrete devices have to meet tighter height requirements.

Stringent size constraints accentuate certain problems, which are present in discrete circuit implementations, such as isolation requirements between filters, while reducing others, such as board layout complexity. The filter isolation is critical, due to the dual transceiver design of the RFIC and the capability of having both transceivers operate simultaneously.

The following figure illustrates the high level block diagram of the radio subsystem.

0-7803-9433-X/05/$20.00 ©2005 IEEE.

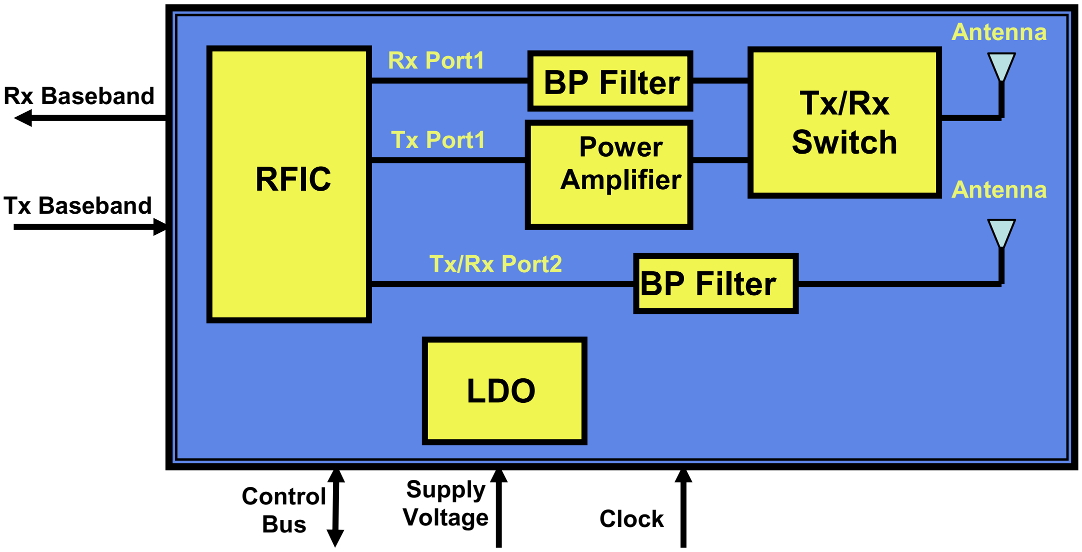


Fig. 1. Radio in a Package (SiP) block diagram

II. System-in-Package Design

This SiP design integrates LDOs, PA, RF switch, decoupling capacitors and bandpass filters with the radio die. An integral overmolded two-compartment shield was used to isolate the PA from the RF receive (Rx) chain, with the intent of also eliminating full system board level EMI shields. The radio die was wire bound, to maintain the same level of parasitics compared to when it was characterized in a package by itself. Power distribution strategy had to be carefully designed to accommodate special requirements, such as the need for separate power pins for the power PA, to minimize propagating power switching transients to the radio circuitry.

The high level of integration of several complex components on this design also increased the complexity of implementing the appropriate Design for Testability (DFT) and Design for Manufacturability (DFM) circuits and capabilities. One useful solution for example, was adding the capability to bypass the internal LDOs for operating at increased voltage levels and for accelerating burn-in tests. In addition, active components were individually powered for increased testability.

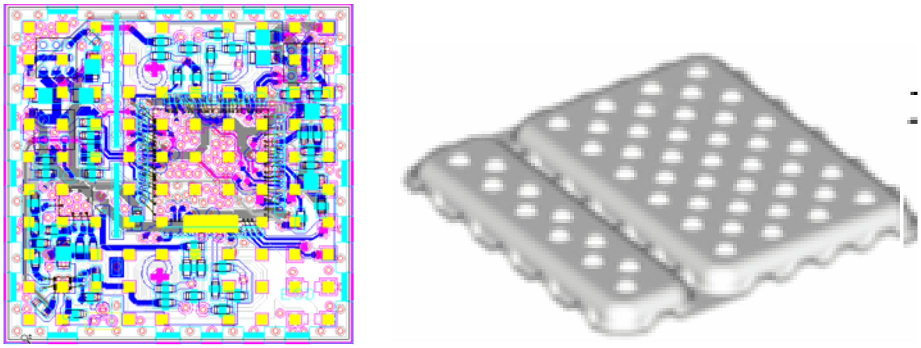


Fig. 2 Radio in a Package (SiP) and shielding structure

For increased yields and cost reductions, a “known-good-die” supply process had to be developed for the bare dies used on the design. This required significant consideration and analysis, since there is a fine balance between the levels of test and cost at die level. A significant element in the design of the embedded filters was the fact that typically the lower Q of embedded inductors increases the insertion loss compared to that of discrete filter implementations.

III. Measurements and Simulations

The proposed Band Pass Filter circuit for 2.4 GHz wireless band, which is composed of the two types of resonator sections, is shown in Fig. 3. One is the series LC resonator, which served as a High Pass Filter function, and the other is the parallel LC resonator, which served as a Low Pass Filter function. In order to reduce the filter size, the series LC resonator and inductance are embedded in the substrate, while the lumped 0201 capacitors are employed for the four capacitances. This new filter has a fourth-order frequency response, but it is much smaller than a microstrip filter, since it is not necessary to layout a microstrip structure with half-wavelength on the substrate. The 3D design model is shown in Fig. 4. The pads on the first layer are designed to launch the four lumped capacitors.

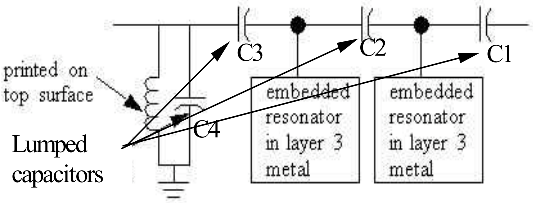


Fig. 3 Schematic of the filter

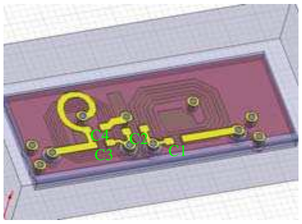


Fig. 4. 3D model of the filter

Four test boards for measurements have been fabricated using Getec* and BT-MG* substrates. The layer stack-up and material properties for Getec and BT-MG are shown in Fig. 5. A pair of 200um-pitch Ground-Signal-Ground microwave probes and an Agilent* 8720D VNA was employed to measure the two-port S-parameters. The frequency range was from 100 MHz to 8 GHz. Two-port calibrations were performed to the tip of the probes and the isolation level was under –90 dB. Measured results for fabricated BPF circuits with the value of C4 varied are shown in Fig. 6 (a)-(b). As the value of C4 is increased, the cutoff frequency becomes lower, and shifts to the left. To improve the electrical performance of the filter and avoid the second harmonic of 2.4 GHz, it is necessary to shift the cutoff frequency to around 4.8-5 GHz. To optimize the filter design, HFSS and ADS simulation tools were employed.

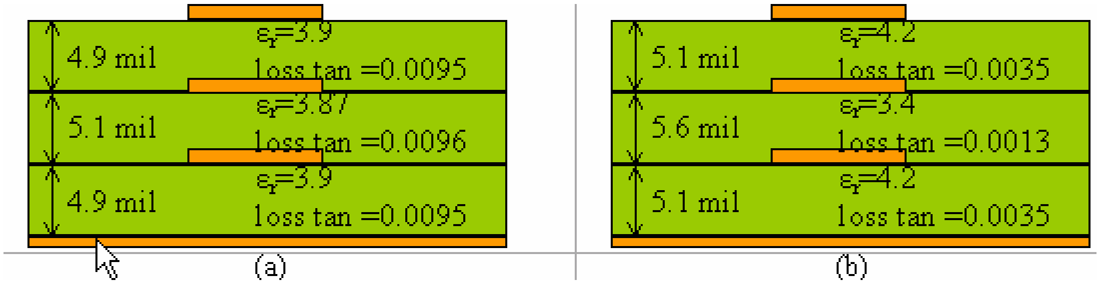
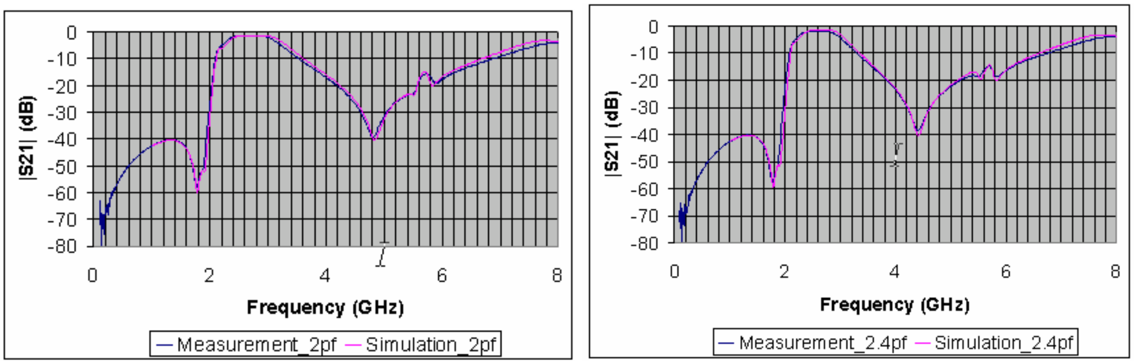


Fig. 5. The stack-up and material properties for Getec and BTMG. (a) Getec, and (b) BTMG.

To simulate the filter designed in Fig. 3, a 3D full-wave modeling tool, HFSS, from Ansoft* was employed. HFSS can account for the copper thickness and the skin effect, compared to ADS*. These effects are very important for a filter design.



(a) (b)

Fig. 6. Measurements vs. simulations. (a) C4=2.0 pf for Getec stack-up and, (b) C4=2.4 pf for Getec stack-up.

Although HFSS can account for lumped elements and their parasitics, it does so at the price of a very long time cycle, since the current version of HFSS will re-mesh every time, even if only the values of the lumped capacitor are changed. Compared to HFSS, ADS can account for the lumped elements and their parasitics in an easier way. To speed-up the optimization, the simulated procedure is divided into two steps. The first step is to use HFSS to simulate the S-parameters of the layout structure only, excluding the lumped capacitors and the associated parasitcs. Then, the simulated S-parameter is imported into ADS, and used as a black box in the schematic, as shown in Fig. 6. In this way, both simulation accuracy and simulation speed can be achieved. Since only the layout structure was modelled in HFSS, the pads for the lumped capacitors were defined as the lumped ports. Thus, the S-parameters for the test structure with 10 lumped ports (two external ports and eight internal ports for the four lumped capacitors) were calculated. To account for the parasitics of the lumped capacitors, the series equivalent circuits for the lumped capacitors have been used for the ADS schematic configurations, as shown in Fig. 6. With different capacitor values of C4, the electrical performances of the filter were simulated. Compared to the measured results, the simulated results show good correlation, as illustrated in Fig. 6. The increased agreements between the measured and simulated results demonstrate the validity of the optimized approach proposed. From these iterations, it can be concluded that the optimized value for C4 is 2.0 pF. As shown in Fig. 5(b), the pass band insertion loss of the optimized filter is about 1.5 dB. The out-of band rejection at 4.8 GHz is better than 35 dB.

Summary:

Careful design considerations, simulations, and manufacturing led to first pass prototypes performing close to initial specifications. The well established design relation between both companies' engineering and their design tools helped to reduce total design and test cycle.