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SFSU Engr 844 - Fall 2008 - Homework 1

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Consider the n-tap FIR example discussed in class:

$$y_n = c_n * x_n + c_{n-1} * x_{n-1} + c_{n-2} * x_{n-2} + \dots + c_1 * x_1$$

given constants $c_n \dots c_1$ and input values x_i at time step i . Unless otherwise specified, assume $n=4$, the number of CPU registers you can use is 128, and that you have a RISC type processor with the following single-cycle instructions:

- LOAD $R_i, M(\text{address})$
- STORE $R_i, M(\text{address})$
- ADD R_{s1}, R_{s2}, R_d
- MUL R_{s1}, R_{s2}, R_d
- MOV R_s, R_d

1. Suppose the current value of x , i.e. x_n , is available through memory-mapped IO at $M(1000)$. In other words, you can access the current value of x by loading from $M(1000)$. The constants are stored in memory location $M(1001) \dots M(1000+N)$. Write the set of instructions that execute one whole loop of the FIR filter. You don't have to worry about the timing of when x_n is read.

Hint: you have to decide which registers correspond to your x 's. Every time the FIR executes, you load just ONE value for x . So you have to somehow remember the old ones. You can assume initially all registers contain 0 (so no need to initialize x 's).

1. How many clock cycles does the first loop of your FIR implementation require? This should include the steps needed to load all necessary data items.
2. Assume each load/store operation takes 10 clock cycles to execute. How many clock cycles does your FIR require?
3. If the processor has a 5-stage pipeline, then how many clock cycles does your FIR require? Remember that now, each pipeline stage executes in 1 clock cycle. Repeat your calculation for the case where memory load/store take 10 instructions.
4. Suppose you now can also use a multiply-accumulate (MAC) instruction:

MAC R_d, R_x, R_c

where $R_d = R_d + R_c * R_x$. Rewrite your FIR implementation to use this new instruction.

5. How many clock cycles does your new FIR require in the non-pipelined and 5-stage pipelined versions? Assume single-cycle load/stores.
2. What is the minimum number of registers required to make your standard and MAC-based implementations work?
3. Suppose registers are very expensive. What is the absolute minimum number of registers required to implement a working FIR? Justify your answer by writing an implementation in assembly using the given instructions. You can assume you have as much memory as you need.
4. Suppose now your processor can perform two MAC operations in a single clock cycle (no other modifications to the register file or memory access). Write a new implementation in assembly to take advantage of this and calculate how many clock cycles it requires to execute.

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execute.

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