

LAB #5: BIPOLAR LOGIC GATES

Updated: Dec. 23, 2002

Objective:

To characterize TTL gates of the 7400 and 74LS00 types. To compare the performance characteristics of the two families, and to justify any differences in terms of internal circuit design.

Components:

1 × 7400 and 1 × 74LS00 TTL Quad 2-Input NAND Gates; 1 × 0.1 μF capacitor, and resistors: 1 × 100 Ω, 1 × 1.0 kΩ, 1 × 10 kΩ, 1 × 100 kΩ (all 5%, ¼ W).

Instrumentation:

A bench power supply, a triangle signal generator, a pulse generator with sharp rise/fall times (1 ns or less), a digital multi-meter, and a dual-trace oscilloscope with low input-capacitance X10 probes.

PART I – BACKGROUND

Even though today’s digital electronics is dominated by CMOS technology, there are still great many systems in operation that were implemented in the bipolar technologies that preceded the takeover by CMOS. Consequently, the servicing and upgrading of these systems requires the knowledge of bipolar logic families, particularly the *transistor-transistor logic* (TTL) and the *emitter-coupled logic* (ECL) families.

The first bipolar logic family to gain widespread acceptance was the 74XX TTL series developed by Texas Instruments around 1965. Its most popular representative is the 7400 Quad 2-Input NAND Gate shown in Fig. 1a. Over the years, this circuit has evolved through a variety of versions aimed at improv-

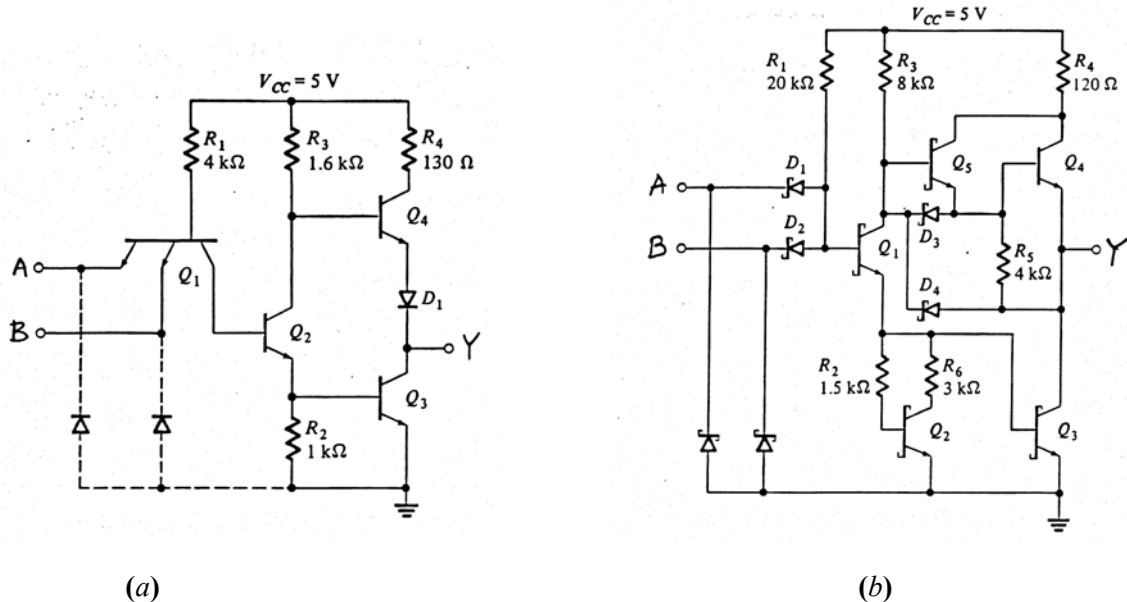


Fig. 1 – Circuit schematics of the 7400 and 74LS00 quad NAND gates

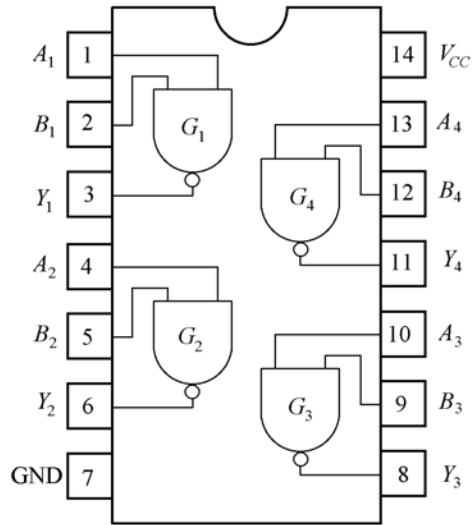


Fig.2 – Pinout for the 7400/74LS00 quad NAND gate.

ing the power-delay product (PDP) as well as other performance figures. A popular descendant, which appeared around 1975, is the 74LS00 Quad 2-Input NAND Gate shown in Fig. 1b. Termed *low-power Schottky* (LS) TTL, it uses larger resistors to reduce power consumption and Schottky barrier diode clamping to prevent BJT saturation and thus improve the propagation delays. Moreover, a redesign of the internal circuitry ensures more symmetric noise margins and output current-drive capability.

PART II – EXPERIMENTAL PART

In this lab we shall characterize both the 7400 and the 74LS00 gates, and compare them against each other to appreciate the improvements brought about by the evolution. You are also encouraged to compare your measurements against the values reported in the data sheets of the two families, which can readily be downloaded from the Web (for instance, by visiting <http://www.google.com> and searching for SN7400 and variants thereof.) The pinout of the quad NAND gates is shown in Fig. 2.

Henceforth, steps shall be identified by letters as follows: **M** for measurements, and **C** for calculations. As you proceed through the various steps, don't forget to take the usual precautions, namely:

- Always turn power off when assembling or modifying a circuit. For simplicity we shall omit showing the power-supply connections, but it is implicit that **Pin # 14 goes to + 5 V, and Pin #7 to ground**
- Always *bypass* the power supply with a 0.1- μ F capacitor mounted as close as possible to your IC.
- Keep leads *as short as possible*.
- Use *low-input capacitance* probes, such as X10 probes.
- Avoid using the digital multi-meter recklessly! Recall that a multi-meter exhibits *low* input resistance when configured as an *ammeter*, and *high* input resistance when configured as a *voltmeter*. As you switch the instrument back and forth between the two modes, avoid creating inadvertent low-resistance connections that might damage both your instrument and your circuit! This occurs if you try to make a *voltage* measurement with the instrument still configured for *ammeter* operation! As a good work habit, always configure your instrument with its terminals *disconnected* from the circuit. Then, for *ammeter* measurements connect it in *series*, and for *voltmeter* measurements connect it in *parallel*.

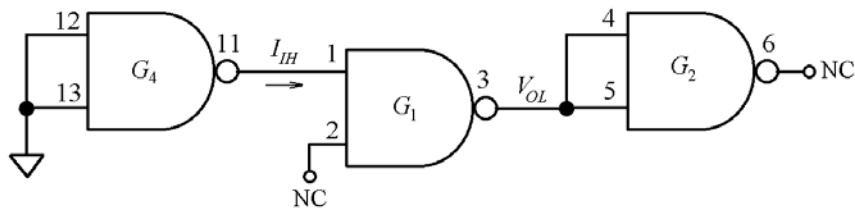


Fig. 3 – Test circuit to measure G_1 's I_{IH} and V_{OL} .

7400 Gates:

In the following we are going to characterize gate G_1 of the 7400 IC for the case in which it drives and is driven by a similar gate.

M1: Mark one of the 7400 ICs available in your kit (the other is a spare), and wire the circuit of Fig. 3 with power off (*NC* stands for *Not Connected*.) Apply power ($V_{CC} = 5.0$ V), and measure I_{IH} and V_{OL} .

Warning: Avoid reckless usage of the multi-meter!

M2: Change the inputs to gate G_4 as shown in Fig. 4, and measure I_{IL} and V_{OH} .

C3: With reference to Fig. 1, calculate the *actual value of Q_1 's base resistance* as $R_1 = (V_{CC} - V_{BE1(on)} - V_{OL})/I_{IL}$, where $V_{CC} = 5$ V, $V_{BE1(on)} \cong 0.7$ V, and V_{OL} and I_{IL} are as measured in Steps M1 and M2. This gives you an idea of how close an actual IC resistance may be to its nominal value (4 k Ω in this case.)

C4: With reference to Fig. 1, find Q_1 's *reverse-active current gain* as $\beta_{R1} = I_{IH}/I_{B1}$, where I_{IH} is as measured in Step M1, and I_{B1} is calculated as $I_{B1} = (V_{CC} - V_{BC1(on)} - V_{BE2(on)} - V_{BE3(on)})/R_1$. Use R_1 of Step C3, and assume junction voltage drops of 0.7 V.

MC5: Assemble the circuit of Fig. 5a, and measure I_{E1} and I_{E2} . With reference to Fig. 1, we note that Q_1 operates in yet another reverse-active mode, with one of its emitters acting as emitter, and the other as collector. Calculate $\alpha_R = I_{E1}/I_{E2}$, and thus $\beta_R = \alpha_R/(\alpha_R - 1)$. Compare with the value of β_R found in Step C4, and justify any difference using physical considerations.

M6: Assemble the circuit of Fig. 5b with the variable source V_S initially set to 0 V. Then, turn on $V_{CC} = 5$ V, and while monitoring V_{C3} with the DVM, **slowly** increase V_S until you obtain $V_{C3} \cong 0.5$ V (don't increase V_S further, as the output transistor Q_3 may end up dissipating excessive power and get damaged!) Finally, measure I_{C3} , the *maximum current* that Q_3 is capable of sinking.

C7: With reference to Fig.1, calculate Q_3 's base current I_{B3} when both inputs to the gate are high (use the nominal resistance values shown, and assume junction voltage drops of 0.7 V and $V_{CE2(sat)} \cong 0.1$ V.) Hence, using I_{C3} as measured in Step M6, estimate Q_3 's *forward-active current gain* as $\beta_{F3} = I_{C3}/I_{B3}$.

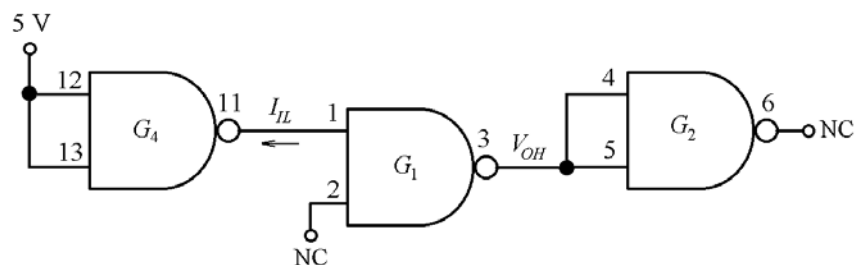


Fig. 4 – Test circuit to measure G_1 's I_{IL} and V_{OH} .

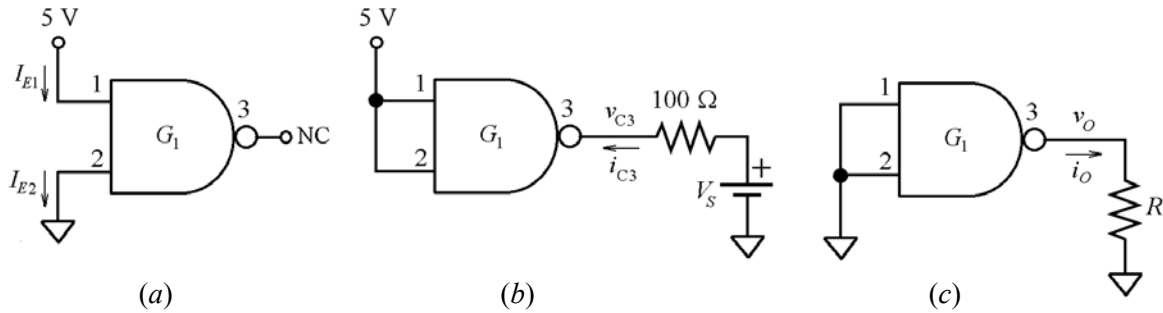


Fig. 5 – Test circuits to: (a) investigate the RA characteristic of the input BJT; (b) measure the current sinking capability of the output BJT; (c) investigate the i - v characteristic with a high output.

M8: Assemble the circuit of Fig. 5c, and measure v_O and i_O for $R = 100\text{ k}\Omega$, $10\text{ k}\Omega$, and $1\text{ k}\Omega$. Hence, using these three data points, sketch and label on grid paper the best-fit v_O - i_O curve.

C9: The 7400 data sheets guarantee a fan-out of 10. However, the results of Steps M2 and C7 indicate that in the *output-low state* your particular gate sample could actually drive many more similar gates, namely, $N = I_{C3}/I_{IL}$. If your gate were to actually drive this many gates, when in the *output-high state* it would have to source the current $I_O = N \times I_{IH}$, with I_{IH} as measured in Step M1. Using the curve of Step C7, estimate the corresponding value of v_O . Can this still be regarded as a reasonable value for V_{OH} ? Explain!

MC10: Using the circuit of Fig. 6, display the VTC of gate G_1 on the oscilloscope. Next, find V_{IL} and V_{IH} graphically, and finally calculate the noise margins NM_L and NM_H .

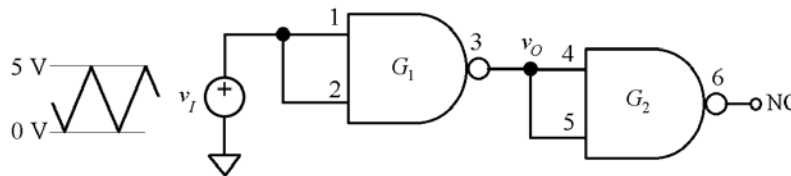


Fig. 6 – Test circuit to display G_1 ' VTC.

MC11: Using the circuit of Fig. 7, measure the propagation delays t_{PHL} and t_{PLH} of gate G_1 for the case in which it drives another similar gate, as shown. Then, calculate its average propagation delay as $t_P = (t_{PHL} + t_{PLH})/2$.

Warning: Use a X10 probe, and beware of probe loading!

MC12: *If time allows*, investigate the degree of *matching* among the four gates of your IC. To this end,

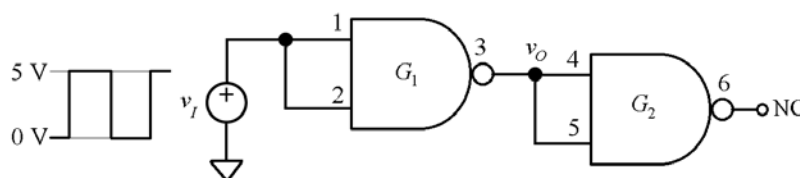


Fig. 7 – Test circuit to find the propagation delays.

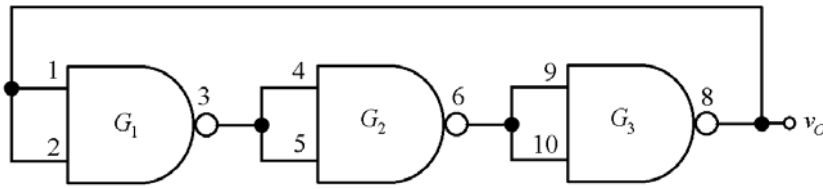


Fig.8 – Ring oscillator.

repeat the characterization that you have just performed for G_1 , but for the remaining gates G_2 , G_3 , and G_4 . Prepare a *table* with the parameter values for each gate as well as their averages, and comment on the *parameter spread* across the four gates.

MC13: Measure the current I_{CC} drawn by your IC from the supply V_{CC} with the inputs to all four gates first connected to ground, then to V_{CC} . Next, calculate the *average power dissipation per gate* as $P = \frac{1}{4}V_{CC} \times I_{CC(\text{avg})}$. Finally, calculate the power-delay product as $PDP = P \times t_P$

MC14: With power off, interconnect three of the gates for *ring-oscillator* operations as in Fig. 8. Next, apply power, measure its period of oscillation T , and then find the average propagation delay as $t_P = T/6$. Finally, compare with that found in Step MC11, and justify any differences.

Warning: Use X10 probes and beware of probe loading!

MC15: Measure the current I_{CC} drawn by the ring counter of Fig. 10, calculate the product $V_{CC} \times I_{CC}$, and subtract from it the power dissipated by the fourth (unused) gate with its inputs high, using the data of Step MC13. The result is the *average power* dissipated by the *entire* ring counter. Dividing this by 3 gives the average power P dissipated by each of its gates. How does this compare with that found in Step MC13? Justify any difference.

74LS00 Gates:

The remainder of the lab is devoted to the characterization of a 74LS00 IC, and its comparison with the 7400 family to appreciate the performance improvements. Before proceeding, mark one of the 74LS00 ICs available in your kit (the other is a spare.)

M16: Retracing Steps M1 and M2, find I_{IH} , V_{OL} , I_{IL} , and V_{OH} for the 74LS00 family, compare with those of the 7400 family, and justify the differences in terms of the circuit schematics of Figs. 1 and 2.

M17: Retracing Step MC10, display the VTC of the 74LS00 family, find V_{IL} and V_{IH} , calculate the noise margins NM_L and NM_H , compare with those of the 7400 family, and justify the differences in terms of the circuit schematics of Figs. 1 and 2.

MC18: Retracing Step MC11, find t_{PHL} , t_{PLH} , and t_P for the 74LS00 family, and compare with the 7400 family.

Warning: Use X10 probes and beware of probe loading!

MC19: Retracing Step MC13, find P and PDP for the 74LS00 family, compare with the 7400 family, and justify the differences in terms of the circuit schematics of Figs. 1 and 2.

MC20: Retracing Steps MC14 and MC15, investigate the ring-oscillator behavior of the 74LS00 family, compare with the 7400 family, and justify any differences in terms of the schematics of Figs. 1 and 2.

Warning: Use X10 probes and beware of probe loading!