Brief Papers

High-Speed, Low-Power BiCMOS Comparator Using a pMOS Variable Load

A. Boni and C. Morandi

***Abstract*— A novel BiCMOS latched comparator for high-speed, low-power applications is proposed. The resistive load of conventional current-steering comparators is replaced by a variable load made by a pMOS transistor that, during the comparison cycle, is successively biased in three different operating regions. This solution provides a lower power consumption than conventional architectures, without sacrificing sampling speed. Post-layout simulation results and measurements performed on the prototypes are presented.**

***Index Terms*— Analog-digital conversion, BiCMOS analog integrated circuits, comparators, high-speed integrated circuits.**

I. Introduction

THE increasing interest for high-speed, low-power, low-voltage A/D converters can be explained by the growth of the market of portable, battery-powered equipment, by the scaling of device sizes, which requires a reduction of supply voltages, and by the shift toward higher frequencies of the boundary between analog and digital signal processing.

The classical latched comparator, in bipolar or BiCMOS technology, Fig. 1, was successfully used in high-speed A/D converters [1], operating without sample-and-hold (S/H). Its intrinsic limits, however, become apparent when the reduction of power consumption and supply voltage is at stake.

This paper discusses the design and implementation of a novel BiCMOS latched comparator [2] featuring 160 Ms/s, 8-b resolution on a 1-V input range, with a power consumption of 340 μW, at a single supply voltage of 3.3 V $\pm$10%. The load resistances of the classical comparator are replaced by pMOS transistors which are successively biased in different operation modes during the three phases of each comparison cycle. By this technique, the comparator always operates with the optimum load, achieving the lowest power consumption without sacrificing the sampling speed. The improvement obtained with respect to conventional architectures is demonstrated by circuit analysis and simulations. The comparator was designed and manufactured in a 1.2-μm BiCMOS technology [3]. The results of the measurements performed on the prototypes confirm the theoretical predictions.

II. High-Speed Latched Comparators: Theory

In order to quickly resolve differential voltages of few millivolts, circuits with positive feedback are commonly used, like the well-known latched comparator of Fig. 1 [1]. Its performance can be improved by an input preamplifier [4]. In order to highlight the limits of this architecture, the circuit behavior must be considered both in the *acquisition* phase ($ck = 1$), when it behaves as a differential amplifier, and in the *regeneration* phase ($ck = 0$), when it exploits positive feedback to reach valid digital levels within half a clock period. With reference to previous works, e.g., [1] and [5], the following five fundamental relationships can be easily obtained, which estimate the *recovery time* ($t_{\rm rec}$), the bandwidth of the differential amplifier ($f_{3\,\rm dB}$), the small-signal regeneration behavior, the low-frequency output swing, and the maximum rate of change at the outputs:

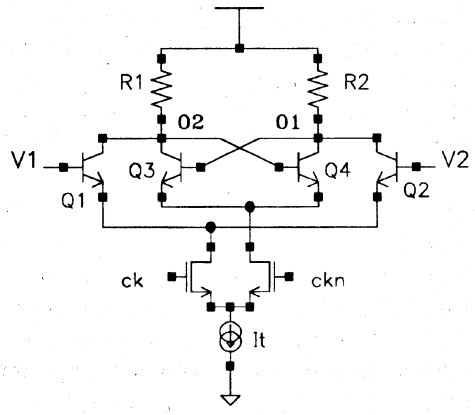

Fig. 1. Circuit diagram of the conventional latched comparator.

$$t_{\rm rec} = R_L C_{T\rm acq} \ln\left[1 + \frac{1}{\tanh(A_p V_{In}/2V_{th})}\right] \quad (1)$$

$$f_{3\,\rm dB} \approx \frac{1}{2\pi r_L C_{T\rm acq}} \quad (2)$$

$$v_{\rm Out} = V_{O1} - V_{O2} \approx A_p A_v v_{\rm In}(t_1) \exp\left(\frac{t - t_1}{\tau_{\rm reg}}\right)$$

with

$$\tau_{\rm reg} = \frac{C_{T\rm reg}}{g_m} \frac{g_m r_L}{g_m r_L - 1} \quad (3)$$

$$|V_{\rm Out}(t = t_2)| \le I_T R_L \frac{\beta - 1}{\beta + 1} \quad (4)$$

$$\left|\frac{dV_{O1/2}}{dt}\right| \le \frac{I_T}{C_{Tsr}}. \quad (5)$$

t_1 and t_2, respectively, mark the falling and the rising edge of the clock, V_{th} is the thermal voltage, $V_{\rm In} = V_1 - V_2$, A_p is the voltage gain of the input preamplifier (if present), $C_{T\rm acq} \approx C_L + 2C_{js} + 4C_{\mu L} + C_{\mu A}$ is the total capacitance affecting

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The authors are with the Dipartimento di Ingegeneria dell'Informazione, University of Parma, I-43100 Parma, Italy.

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the acquisition phase[1] (C_L being the load capacitance, C_{js} the substrate-collector junction capacitance of Q1–Q4, $C_{\mu A}$ and $C_{\mu L}$ the base–collector junction capacitance of Q1,2 and Q3,4, respectively), r_L is the small-signal load resistance (R_L in Fig. 1), A_v is the small-signal gain of the differential amplifier Q1,2, g_m is the transconductance of Q3,4, $C_{Treg} \approx C_\pi + C_L + 2C_{js} + 4C_{\mu L}$ is the capacitance affecting the regeneration operation (C_π being the total base–emitter capacitance of Q3,4), β is the current gain of Q3,4 and $C_{Tsr} \approx C_L + 2C_{js} + 4C_{\mu L} + C_{je}$ (C_{je} being the base–emitter depletion capacitance of Q3,4). Equations (1) and (2) refer to the *acquisition* phase, while (3)–(5) refer to the *regeneration* phase. In order to avoid bit errors, to attenuate the third harmonic distortion of the whole analog-to-digital converter (ADC) (related to the frequency and amplitude limitation in the comparator [6]) and to achieve a sufficient output voltage swing, all the five fundamental equations should be simultaneously taken into account. Note that, provided constraint (5) is met, a wider voltage swing and a smaller $\tau_{\rm reg}$ can be achieved by increasing the value of R_L, but this is often not compatible with constraints (1) and (2) at high frequencies. In fact, *regeneration* and *acquisition* pose conflicting requirements on the load resistance, so that higher sampling frequencies can only be achieved by increasing current consumption.

III. The Variable Load Comparator

Modifications of the scheme of Fig. 1, such as cascoding [7] or load resistor splitting [8], were proposed in order to improve dynamic performance, but no one leads to significant power savings and is compatible with the reduction of the supply voltage. The *variable load latched comparator*, proposed in Fig. 2, is an evolution of the conventional scheme, where pMOST's M1,2 switched from saturation to nonsaturation, replace load resistors R1,2, overcoming the intrinsic limits of the conventional architecture. The key idea is that the conflicting requirements posed by regeneration and acquisition upon the load resistance can be easily met by controlling the voltage at cl with the three-level waveform, of Fig. 3(a), synchronized with the clock. The comparator can, thus, operate in each phase with the optimum load, and power consumption is minimized without sacrificing the sampling speed.

The waveform in Fig. 3(a) has three levels: 0, V_{tr}, and $V_{\rm reg}$, corresponding, respectively, to reset, tracking, and regeneration. Considering reset at first, (1) predicts that a shorter $t_{\rm rec}$ can be achieved by lowering the load resistance, i.e., by pulling down to ground the gate of the pMOS loads for, e.g., $T_{ck}/4$. For a correct operation in tracking mode, V_{cl} should be then increased to V_{tr}, in order to achieve the required voltage gain and bandwidth. Note that this latch operates correctly with a quite limited amplifier gain (about 1.5), unlike conventional schemes, which require higher gains (5–10, often obtained by a preamplifier [4]): this leads to lower consumption and smaller input capacitance. At $t = t_1$ the gate voltage of the loads is further increased to $V_{\rm reg}$, in order to increase the small-signal load resistance. Fig. 3(b) shows the simulated output of

[1]It should be noted that the expression of $C_{T\rm acq}$ used here differs from (11) in [5].

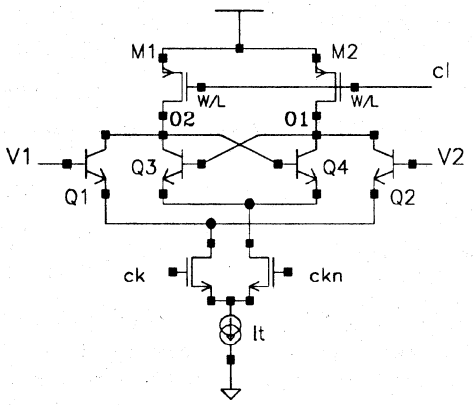
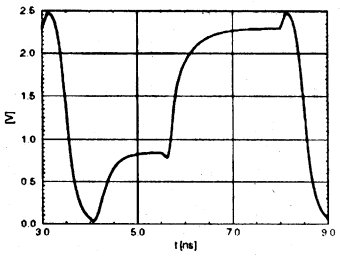
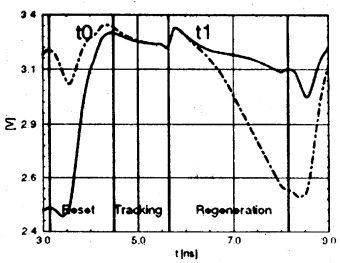


Fig. 2. Circuit diagram of the *variable load latched comparator*.



(a)



(b)

Fig. 3. Simulated (a) V_{cl} and (b) $V_{\rm Out}$ of the variable load comparator in a comparison cycle.

the comparator, sampling the smallest input voltage, i.e., 1/2 least significant bit (LSB). Three subphases can be recognized during *regeneration*. At first, both V_{O1} and V_{O2} increase suddenly because of the capacitive coupling with the cl line, then both decrease, due to the increased load resistance, and positive feedback regenerates the initial output voltage $V_{\rm out}$, according to the linear model of (3), with a $\tau_{\rm reg} \approx C_{Treg}/g_m$, thanks to the high resistance provided by M1,2. In the third subphase of regeneration, one of the two bipolar junction transistors (BJT's), say Q3, is turned off, and from this instant, t_1', V_{O1} decreases linearly with time, while V_{O2} settles not far from $V_{\rm dd}$. The large signal behavior of the comparator can then be analyzed with the simplified schematic of Fig. 4, where M1 is modeled as a quasi-linear resistor, M2 as a current source and only depletion capacitances were retained for Q3, turned off. By balancing currents at node O1 and neglecting the voltage drop across M1, the following relationship is obtained:

$$V_{O1}(t) = V_{O1}(t_1') - \frac{I_T - I_L}{C_L + 2C_{js} + 2C_{\mu L} + C_{\mu A} + C_{je}} \cdot (t - t_1') \quad (6)$$

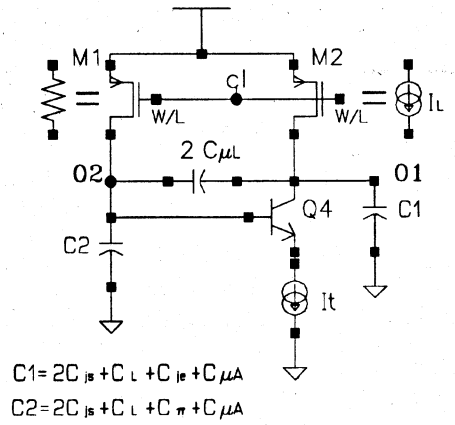


Fig. 4. Simplified circuit diagram for transient analysis.

where I_L is the saturation current of M2. Since V_{O2} is nearly constant, the differential output voltage $V_{\rm Out}$ decreases linearly with time and, therefore, *the output swing of the variable load comparator can be made larger without any increase of the current consumption by reducing the value of* I_L, i.e., *by increasing* $V_{\rm reg}$. However, (6) and the simplified schematic of Fig. 4 hold as long as the current through M1 is appreciably smaller than I_L, otherwise, M1 saturates and V_{O2} decreases quasi-linearly with time. To avoid this, I_L should be greater than

$$I_{L\,\min} \approx I_T \frac{2\,C_{\mu L}}{C_L + 2\,C_{js} + 4\,C_{\mu L} + C_{\mu A} + C_{je}} \qquad (7)$$

as may be found by current balancing at node $O2$. Since simulation shows no increase in the final aperture $V_{\rm Out}(t_2)$ for $I_L < I_{L\,\min}$, $V_{\rm reg}$ should be set so that I_L is only slightly higher than $I_{L\,\min}$. In fact, if I_L is made smaller than $I_{L\,\min}$, e.g., by setting $V_{\rm reg}$ to $V_{\rm dd}$, the settling time of output nodes is significantly increased together with power consumption.

On the basis of this discussion it appears that a simpler solution, using a two-level waveform, would not be as effective as this in minimizing power consumption. Elimination of the intermediate level V_{tr} would in fact reduce too much the gain of the comparator in acquisition mode, forcing the adoption of an input preamplifier. The circuit proposed in [5] with a time varying load driven by *ckn* actually requires a higher bias current and an emitter coupled logic (ECL) latch to obtain an acceptable voltage swing, at the cost of higher power consumption.

A simple circuit for generating the waveform of Fig. 3(b) is shown in Fig. 5, where $V_{\rm reg}$ and V_{tr} can be easily obtained by on-chip references. Simulations prove that a 10% tolerance on $V_{\rm reg}$ and V_{tr} and a ± 125 ps error in the edges of the waveform driving M1–2 do not affect the performance of the comparator. The power required for driving M1,2, represented by $C_{\rm load}$, is

$$P_{\rm load} = C_{\rm load}\, f_{ck}\, V_{\rm reg}^2 + P_{\rm ref} \qquad (8)$$

where $P_{\rm ref}$ is the power dissipated in the on-chip level-shifters used to obtain $V_{\rm reg}$ and V_{tr} from $V_{\rm dd}$. In the specific case, at 160 Ms/s and 3.3-V supply, $P_{\rm load}$ corresponds to about 140 μW.

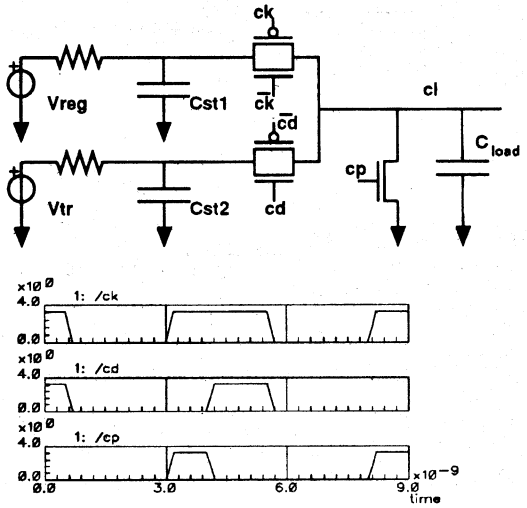


Fig. 5. Circuitry of the three-level waveform generator used to drive the gate of M1 and M2.

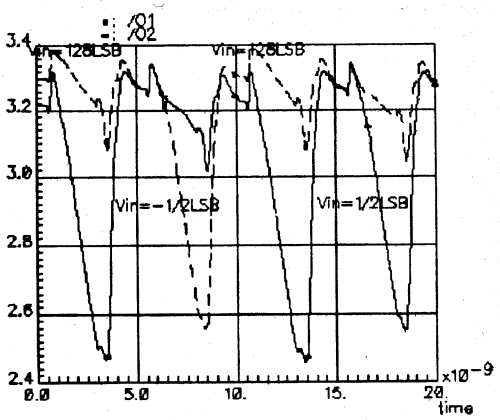


Fig. 6. Output voltage waveforms of the proposed comparator obtained from a post-layout simulation.

In order to convert the small swing positive ECL (PECL) levels at $V_{O1} - V_{O2}$ to full CMOS levels, a cascade of two low-kickback, current starved, dynamic CMOS flip-flops dissipating only 390 μW at 160 Ms/s was used.

IV. Simulations and Experimental Results

Fig. 6 shows the post-layout simulated output waveforms V_{O1} and V_{O2} of the proposed comparator, sampling at 200 Ms/s a differential input switching at 100 MHz between 128 LSB (0.5 V) and $\pm$1/2 LSB ($\pm$1.95 mV), which is a commonly accepted worst case input stimulus for a latched comparator [5], [9]. A level 15 MOS model was used; all the parasitic capacitances and the load represented by the CMOS flip-flop were included, and a 1.3 σ mismatch in the pMOS loads was considered, according to the process tolerances. The tail current was set to 60 μA: this plus the mean current drawn by the *cl* line (30 μA at 200 Ms/s, 3.3-V supply) should be compared with 200 μA required by a conventional comparator designed with the same technology and featuring the same sampling speed and resolution.

With worst speed device parameters (2σ), a sampling frequency of 160 MHz is achieved with a tail current of 70 μA

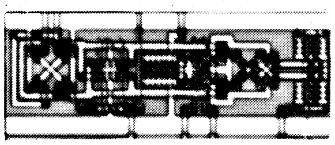


Fig. 7. Photograph of the silicon prototype.

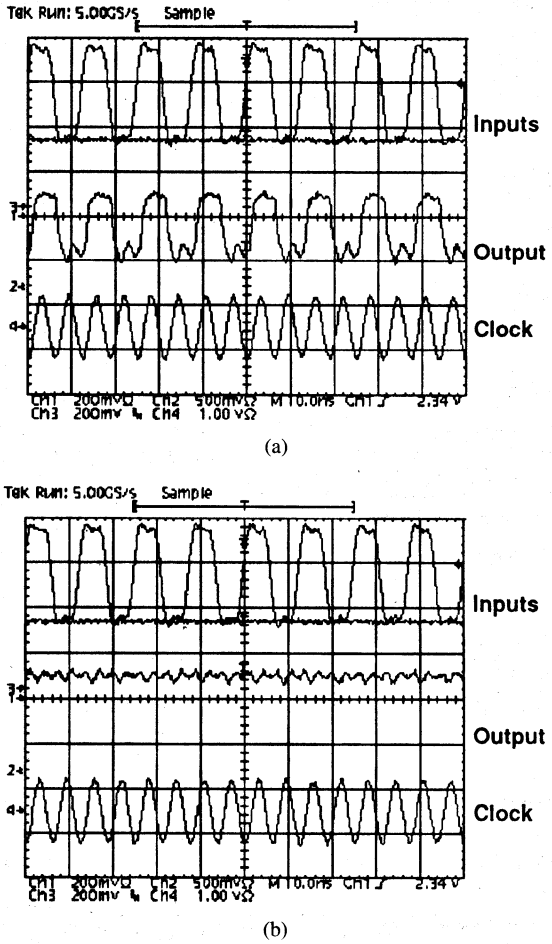


Fig. 8. Oscilloscope's screen showing the signals at the input of the comparator, the output signal and the clock. The constant input signal was shifted by 2 mV to switch from situation (a) to situation (b).

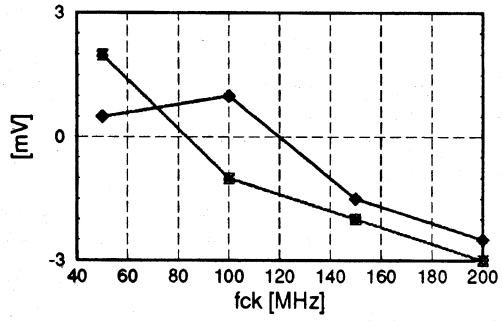


Fig. 9. Measured input offset voltages of two samples.

and forcing the V_{tr} and V_{reg} levels to track the run-to-run variations of the pMOST's parameters by means of on-chip references. The proposed comparator was implemented in a 1.2-μm BiCMOS technology [3]. The photograph of the prototype, 190 $\times$ 71 μm^2 in size, is shown in Fig. 7.

TABLE I
SPECIFICATIONS OF THE VARIABLE LOAD COMPARATOR

Technology	1.2μm BiCMOS
Comparator cell size	190x71μm²
Max. Sampling Freq.	160MHz
Input Offset Voltage	≤2mV
Supply Voltage	3.3V±10%
Power Consumption at 160Ms/s	
Input Followers	200μW
Latched Comparator	340μW
CMOS Interface	390μW

Measurements, performed at the maximum sampling speed, 160 Ms/s, and with a maximum frequency square wave input (80 MHz), are shown in Fig. 8, which reports the input stimuli, the output (converted to PECL levels), and the sinusoidal clock (in-chip converted to CMOS levels). In both situations, the comparator is subject to a large overdrive each second clock period. In order to move from situation (a), where the comparator's output changes with a frequency of $f_{ck}/2$, to (b), where the output is stuck at the high level, the constant voltage at the comparator's negative input was changed by 2 mV, i.e., 1/2 LSB. The input offset voltage, measured with dc input signals, at different sampling frequencies, is within ± 2 mV (1/2 LSB for 8-b on 1-V differential range) up to 150 MHz, Fig. 9. A summary of the specifications of the proposed comparator is reported in Table I.

V. CONCLUSIONS

A novel BiCMOS comparator featuring 160 Ms/s with 3.3-V $\pm 10\%$ supply and dissipating 340 μW was presented. This comparator makes use of pMOS loads, whose operating region is changed three times during the comparison cycle, providing high sampling speed together with reduced power consumption. The advantages of the proposed architecture were demonstrated by circuit analysis and simulations and confirmed by measurements on the prototypes.

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